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Electronics based on two-dimensional materials

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The compelling demand for higher performance and lower power consumption in electronic systems is the main driving force of the electronics industry's quest for devices and/or architectures based on new materials. Here, we provide a review of electronic devices based on two-dimensional materials, outlining their potential as a technological option beyond scaled complementary metal-oxide-semiconductor switches. We focus on the performance limits and advantages of these materials and associated technologies, when exploited for both digital and analog applications, focusing on the main figures of merit needed to meet industry requirements. We also discuss the use of two-dimensional materials as an enabling factor for flexible electronics and provide our perspectives on future developments.

The shrinking of the geometrical dimensions of planar devices[1], plus the introduction of additional performance boosters such as strain, high-k gate dielectrics (where k is relative dielectric constant) and metal gates, have been successful approaches for improving transistor performance in the past 60 years (ref. 2). Furthermore, the semiconductor industry has taken advantage of the third dimension by putting into production the tri-gate transistor[3] illustrated in Fig. 1a for the 22-nm node[4]. Together with planar ultrathin body (UTB) technology[5] (Fig. 1b), three-dimensional (3D) devices represent an alternative to bulk planar technology, which may not provide significant performance improvements below the 22-nm node. Indeed, in bulk planar devices, good electrostatic control of the channel by the gate voltage requires prohibitively thin gate oxides, which leads to increased leakage, to very high substrate doping and eventually to charge carrier mobility (μ) degradation. In the case of tri-gate and UTB transistors, however, issues related to leakage and doping levels are mitigated.

Sustaining Moore's law[6] has therefore required, in the past 10 years, the adoption of new device geometries and of new materials. The current International Technology Roadmap for Semiconductors (ITRS)[7], which assesses the technology requisites for the next-generation semiconductor devices and processes for complementary metal–oxide–semiconductor (CMOS) technology, predicts that additional new materials and transistor geometries will be needed to successfully address the formidable challenges of transistor scaling in the next 15 years (ref. 7).

Two-dimensional materials (2DMs), that is, transition metal dichalcogenides (TMDs), Bi_2Se_3 and Bi_2Te_3, as well as graphene, provide the option of ultimate thin 'channel' transistors and the opportunity for new device concepts (Fig. 1c). The ability to control the channel thickness at the atomic level translates into improved gate control over the channel barrier and into reduced short-channel effects, which are one of the main issues in ultrascaled devices, together with high fabrication costs and power consumption.

The isolation of graphene in 2004–05 by the Manchester group[8,9] has paved the way to the rediscovery of many other 2DMs, semiconducting and metallic, such as TMDs with a general chemical formula of MX_2, where M is a transition metal atom (for example, Mo, W, Ti, Zr, Ta, Nb) and X is a chalcogen atom (for example, S, Se, Te). For example, the crystal structure of molybdenite monolayers was already studied in 1923 by Dickinson and Pauling[10], and monolayer MoS_2 was investigated[11] in 1986. TMD materials have the advantage over graphene of having extended bandgap tunability through composition, thickness and possibly even strain control[12,13]. The proper selection of promising materials for electronics will require basic understanding of the electrical properties, as well as structural information so as to allow heterostructure design[14] with desired properties and with the concrete prospects to produce reliable devices for high-volume manufacturing.

In this Review, we will discuss the current status of the most promising 2DM-based electronic devices, and their prospects for the development of next-generation devices within a mid- to long-term perspective. To this purpose, we will focus on 2DM-based technology for future CMOS devices, not addressing proof-of-concept devices (for example, those based on transport of spin, excitons and so on), which have been recently and widely discussed by Nikonov and Young[15]. Many of these still have to be experimentally demonstrated.

Challenges in electronic-grade 2D materials processing

Although devices based on 2DMs have been produced by exfoliation from the bulk counterpart using a variety of techniques[8,16], production processes with 'on-demand' tuning of structural and electronic properties have not yet been achieved. Growth of large-area[17,18], high-quality[18,19], single-crystal 2DMs, required for the practical realization of 2DM-based technologies and for high-volume manufacturing, is perhaps one of the most challenging tasks. To control materials at the monolayer level the nucleation phenomena and associated surface science and defect control needs to be understood at a level so far not demonstrated in any other multicomponent materials system.

Graphene[8,9] can be grown on several metal substrates[17,19], and progress is being made towards large-area single crystals (up to ~1 cm)[18] made by chemical vapour deposition (CVD) on Cu substrates[19]. It has also been found that the substrate has a large effect on the transport properties: specifically, the μ of CVD graphene transferred onto multilayer hexagonal boron nitride (h-BN) is comparable to that of exfoliated graphene, 10^4 to 3×10^4 cm^2 V^{-1} s^{-1} (refs 18,20) at room temperature[7,21]. There are now ongoing efforts in growing graphene directly on dielectric surfaces such as h-BN

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and other dielectrics[22,23]. Although low-temperature graphene growth has been shown on MgO (ref. 24) and Cu foils, by thermal (300 °C)[25] and microwave CVD (285 °C)[26], its suitability for electronic applications has yet to be demonstrated. Figure 2 shows that the mobility of graphene grown at high temperature (~1,000 °C) is superior to that grown at low temperatures (~300 °C).

Graphene has also been grown on SiC (refs 27–29), and its quality has been shown in ref. 30 to be strongly dependent on the growth and annealing conditions. As the cost of SiC is still high in comparison with Si (http://www.tankeblue.com/news_55_en.html), if the growth of graphene on SiC were the only way to achieve beyond-CMOS devices then the industry would have to re-evaluate the economic viability of such an approach.

Chemical vapour deposition is being evaluated to grow other 2DMs such as h-BN (ref. 31), and TMDs such as MoS_2 (refs 32,33) and WS_2 (ref. 34). The critical parameters that have to be controlled for the preparation of electronic-quality films are stoichiometry, doping, thickness, crystallographic orientation, grain or domain size, and surface roughness. TMD monolayer and few-layer film growth processes are still in their infancy, and many groups around the world are investigating ways of producing them. Growth of high-quality TMDs requires careful control of thickness, purity and point defects, such as chalcogen vacancies, which can be detrimental to transport properties. Point defects in TMDs are controlled by specific thermodynamic conditions such as crystal temperature and chalcogen vapour pressure[35], given that the vapour pressure of the chalcogen is high at the growth temperature[36] used by most of the growth techniques used so far, such as vapour transport epitaxy and CVD.

To reduce the effect of the chalcogen vapour pressure during the growth of TMD materials, lower-temperature growth techniques, such as molecular beam epitaxy (MBE)[37] and atomic layer deposition (ALD), could be used. Molecular beam epitaxy has traditionally been used to grow multicomponent heterostructures of II–VI, III–V and metal oxide materials, whereas ALD has been used to deposit dielectric and metal films. Molecular beam epitaxy can enable the growth of TMD heterostructures by allowing the individual components to be chosen on demand[38,39], thus achieving 'good-quality' films on different substrates. However, there are not enough data yet to judge or comment on the advantages and disadvantages of the technique[40]. Atomic layer deposition (or epitaxy), although a possible growth technique for 2DMs, has received much less attention than MBE mainly because of the difficulty in precursor design and selection.

Two-dimensional materials can also be produced by liquid-phase exfoliation (LPE)[41–45] of their bulk counterpart. This top-down approach is the starting point for large-scale and reliable production of printable devices, but it is still at an early stage of development[44]. The development of LPE is of critical importance for the fast-growing market of printed and flexible electronics[46], which is expected to reach US$76 billion by 2023 (http://www.idtechex.com). The structural and electronic quality of LPE-prepared 2DM films is significantly lower than that obtained by micromechanical cleaving[8,9,16,47] or CVD[17–19,31,32,34,48], but there is a significant economic advantage to such an approach for a number of applications, for example, thin-film transistors[44] and radiofrequency (RF) tags, energy applications[49], and photonic and optoelectronic devices[50]. Two-dimensional-materials-based inks, for example, have to be developed with on-demand formulations required for ink-jet printing[44,45]. Printable 2DM inks can open up new applications and markets, enabling economically viable device manufacturing. Moreover, ink-jet printing could also be used to create heterostructures of the various 2DMs on demand[51]. For many 2DMs (for example TMDs and metal oxides) intercalation of alkali metals such as Li is, at present, the most effective exfoliation route[52]. But this process suffers drawbacks related to sensitivity to ambient conditions and structural changes in the 2DMs following intercalation[53]; thus LPE[43] could be a preferred exfoliation technique for nanoelectronics applications if sorting processes[42,53,54] guarantee reliable control over the lateral size[42] and thickness[54] of the nanosheets.

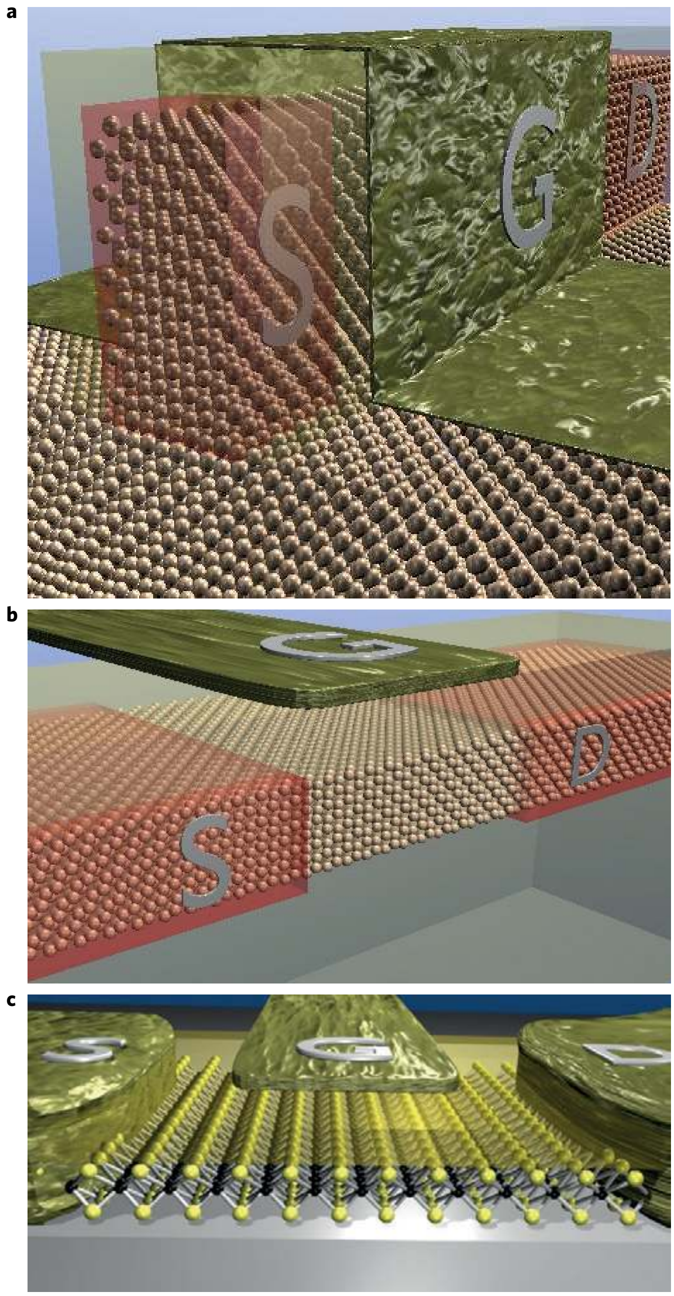

Figure 1 | Sketch of new generation devices. a, Tri-gate device. **b**, Ultrathin body device. **c**, 2DM-based device. In **a**,**b**, individual silicon atoms are visible at these length scales. In **c**, single-layer MoS_2 is the channel material. Doped source (S) and drain (D) are considered and highlighted in red in **a**,**b**, whereas metallic contacts are shown in **c**. The transparent yellow layer represents the oxide. Gate (G) is metallic.

Another crucial point in the fabrication of electronic devices is related to the contact between 2DMs and metals, which needs to be ohmic and have low resistance, as required by the ITRS to comply with performance requirements (total parasitic series source–drain resistance of ~130 Ω μm)[7], as a high parasitic resistance will

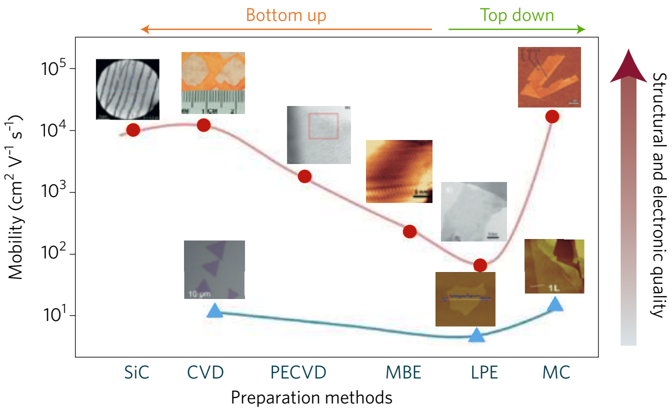

Figure 2 | Mobility of 2DMs as a function of preparation method. Images from left to right (red curve): Low-energy electron microscopy image of graphene grown on silicon carbide[28]; graphene grown by CVD on Cu, the optical image shows the centimetre-scale graphene domains[18]; high-resolution transmission electron microscopy (HRTEM) image showing graphene grown by plasma-enhanced CVD (PECVD)[48]; scanning transmission microscopy image of graphene grown by MBE[25]; HRTEM image of graphene films prepared by LPE[44]; and an atomic force microscopy (AFM) image of graphene prepared by micromechanical cleavage (MC)[8]. The red curve shows the mobility of graphene on SiO_2, data from refs 18,29,44,47,48, and the blue curve is for MoS_2 on SiO_2, data from refs 45,77,78,86,142, extracted from FETs. The mobility of graphene depends on the preparation method. Although temperature is not explicitly indicated, graphene grown at high temperatures (for example, on SiC (ref. 29), by CVD[18], PECVD[48] and MC[47]) has a higher mobility than that grown at lower temperatures (for example, by MBE[25], LPE[44]). The mobility of MoS_2 is less dependent on the preparation process (blue curve; images from left to right: optical micrograph of MoS_2 made by CVD[33]; AFM image of MoS_2 made by LPE[45]; AFM image of MoS_2 made by MC[86]). Images reproduced with permission from: SiC, ref. 28, 2009 Nature Publishing Group; CVD (top), ref. 18, © 2013 The American Association for the Advancement of Science; CVD (bottom), ref. 33, © 2013 American Chemical Society; PECVD, ref. 48, © 2010 American Institute of Physics; MBE, ref. 25, © 2012 American Institute of Physics; LPE (top), ref. 44, © 2012 American Chemical Society; LPE (bottom), ref. 45, 2014 Nature Publishing Group; MC (top), ref. 8, © 2005 National Academy of Sciences, USA; MC (bottom), ref. 86, © 2012 American Chemical Society.

limit the overall device performance. Much effort has been dedicated to the improvement of the contact resistance between metals and 2DMs[55–59], with surface contamination being one of the main causes of high contact resistance[60]. Many attempts have been made to minimize graphene surface contamination, for example, by using high-temperature vacuum annealing, or surface treatments using ozone[61] or oxygen plasma, where in the last case the contact is made on a clean top surface, with the contact at the edge affected by defects caused by the plasma treatment[62]. An alternative route for the 2DM–metal contact, avoiding the surface contamination issue, could be the use of a pure edge contact to graphene (that is, one-dimensional electrical contact to 2DMs)[63]. For 2DMs having a bandgap, the contact must be a metal with a proper work function so that a Schottky barrier is not formed[58,59,64].

Figures of merit

Whenever investigating a new technology for electronic applications, it is of primary importance to define the key figures of merit (FoM) and compare them against the requirements of the ITRS[7]. In particular, here we will focus on the FoM of the two main applications in electronics: digital and analog.

In digital applications, the transistor has the function of a switch (Fig. 3a), that is, two terminals (source and drain) have to be short-circuited or open-circuited, whenever a voltage larger than the 'threshold' voltage (V_T) is applied to the third terminal (the gate). In a circuit, the voltage applied to the terminals (gate, source and drain) can only be swept between 0 and the supply voltage V_{DD}. If we define I_{DS} as the source-to-drain current, V_{GS} as the gate-to-source voltage and V_{DS} as the drain-to-source voltage, I_{off} is the 'off' current (open switch), formally defined as the I_{DS} current when the largest voltage between the source and the drain ($V_{DS} = V_{DD}$) is applied, with no voltage at the gate ($V_{GS} = 0$ V). I_{on} is the 'on' current (closed switch), defined as the I_{DS} current when V_{DD} is applied both to the drain and the gate ($V_{DS} = V_{GS} = V_{DD}$; Fig. 3b). Ideally, one would like to minimize I_{off}, which is proportional to the standby power consumption (that is, power consumed when circuits perform no operation), and to maximize I_{on}, which would provide high switching speed. The I_{on}/I_{off} ratio is a widely used figure of merit for device engineers, and needs to be larger than 10^4 (ref. 7) for future device generations. In Table 1, we report the main FoM extracted from the ITRS 2012[7] for the current technology node (2014) together with the mid- (2018) and long-term (2026) technologies, both for high-performance and low-power applications.

Devices for high-performance applications have large switching speed at the cost of high power dissipation, even in standby. In contrast, low-power applications require devices with low power consumption, a key requirement in portable electronics.

There are intrinsic physical limitations to the maximum I_{on}/I_{off} ratio obtainable for a given supply voltage. At best, I_{DS} increases exponentially from I_{off} to I_{on}, with a rate described by the so-called subthreshold swing (SS), generally expressed in mV dec^{-1} (mV of incremental gate voltage required to change the drain current by one decade). The SS represents the inverse slope of the curve shown in Fig. 3b, a plot of log I_{DS} versus V_{GS}. The smaller the SS, the better the transistor behaves as a switch. In ideal thermionic devices, the intrinsic limit for SS at room temperature is 60 mV dec^{-1} (ref. 65), while SS <60 mV dec^{-1} can be obtained in tunnel devices, where carrier transport is due to interband tunnelling[66]. Obtaining small SS over a wide range of V_{GS} is extremely important, because it implies a large I_{on}/I_{off} ratio at small supply voltage.

Dynamic power consumption (P_D) of a CMOS integrated circuit is proportional to fCV_{DD}^2, where f is the clock frequency and C is the transistor gate capacitance. As a consequence, one of the most effective options to reduce power dissipation is to use a lower power supply voltage, as shown in Fig. 3b. A reduction of P_D is beneficial both for longer battery duration and for ease of heat dissipation in electronic devices.

Another important figure of merit related to device speed is the intrinsic delay time (τ), defined as $\tau = CV_{DD}/I_{on}$; this parameter is linked to the time required to switch a logic gate. Energy consumption per operation is instead considered through the dynamic power indicator DPI = CV_{DD}^2, which is a measure of the energy needed to switch a logic gate. For analog applications, the main FoM are represented by the cut-off frequency (f_T) and the maximum oscillation frequency (f_{max}).

In particular, for frequency lower than f_T, the transistor is able to provide current gain larger than 1, whereas for frequency lower than f_{max}, the power gain can be larger than 1 (the gain for an electrical signal is defined as the ratio between input and output). Let us stress that the power gain is the most relevant gain for actual circuit performance. In analog electronic applications, we need to operate at frequencies for which the transistor is able to deliver a power gain. For example, given the equivalent circuit for the transistor in Fig. 3c, where R_G, R_S and R_D are the gate, source and drain series resistances, respectively, C_{GS} and C_{GD} are the gate-to-source and gate-to-drain

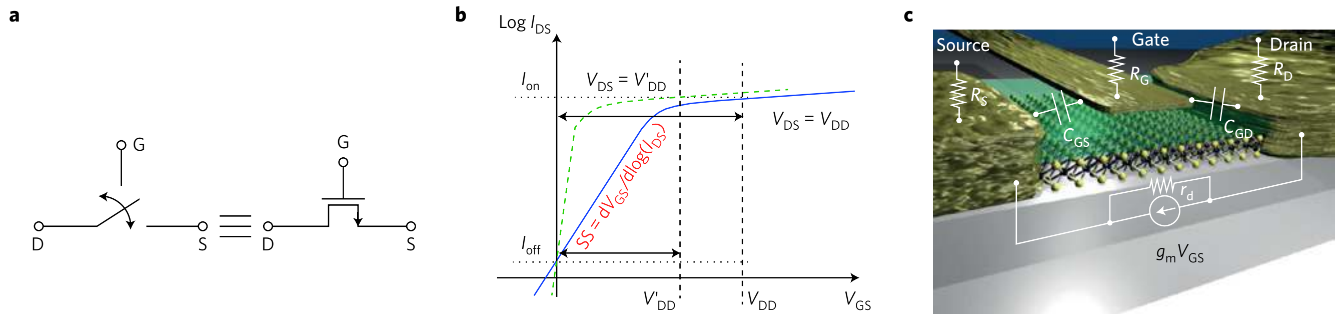

Figure 3 | Digital switch and transistor for analog applications. a, Sketch of the metal–oxide–semiconductor (MOS) transistor acting as a digital switch. **b**, Sketch of the transfer characteristics (I_{DS} versus V_{GS}) drawn on a semi-log scale for different power supplies (V_{DD}, blue curve; and V'_{DD}, dashed green line). The two arrows describe the width of the interval across which V_{GS} is swept, that is, V_{DD} and V'_{DD}. **c**, Sketch of a two-dimensional MOS transistor. The small signal circuit elements are labelled. The transconductance is defined as $g_m = \Delta I_{DS}/\Delta V_{GS}$ at constant V_{DS}, while the output resistance is defined as $r_d = \Delta V_{DS}/\Delta I_{DS}$ at constant V_{GS}.

capacitances, r_d is the output differential resistance (at constant V_{GS}) and g_m is the transconductance, f_{max} can be expressed as[67]:

$$f_{max} = \frac{f_T}{2\sqrt{\dfrac{R_G + R_S}{r_d} + 2\pi f_T R_G C_{GD}}} \quad (1)$$

To improve f_{max}, the series resistance needs to be reduced and large r_d has to be achieved, which is intrinsically obtained in standard silicon or III–V devices, where current saturation is observed in the output characteristics (that is, the current remains almost constant as a function of V_{DS} for a given V_{GS}).

Digital applications

In this section, we will present and comment on the challenges of using 2DMs for digital electronics, both for high-performance and low-power applications in comparison with Si, Ge and III–V-based devices.

High-performance devices. Apart from the main technological challenges in geometric scaling, a bigger intrinsic challenge is provided by material properties: μ in silicon strongly decreases with body thickness reduction or increased doping, undermining possible improvements in device switching speed. However, in the case of tri-gate or UTB transistors, doping levels are much lower[68]. Alternative materials, such as InGaAs or other III–V materials for nMOSFETs, germanium for pMOSFETs, and more strongly strained silicon, are being explored to increase the channel μ for thin body transistors in the 10-nm range[69].

In this context, 2DMs with their extreme thinness can be an alternative. Considering digital electronic applications, graphene field-effect transistors (FETs) cannot comply with ITRS requirements because of the zero bandgap, which leads to at most a few tens I_{on}/I_{off} ratio[70], and large I_{off}. The main specific advantage of TMDs over graphene is the existence of a gap that is in the range ~1–2 eV for most of them, which ensures that they behave as switches with low I_{off}. MoS_2-channel FETs have been fabricated with large I_{on}/I_{off} ratio (>10^4) and small SS (<80 mV dec^{-1}; ref. 16), approaching the desired metric of FETs for CMOS digital circuits. The energy gap of TMDs comes, however, at the cost of low μ (refs 71,72), comparable to that of silicon (few hundreds of cm^2 V^{-1} s^{-1}) and much smaller than that obtainable with III–V materials, for example (few thousands of cm^2 V^{-1} s^{-1})[73], and with graphene deposited over an insulating substrate (>10^4 cm^2 V^{-1} s^{-1})[17,18,20,74,75] (Fig. 4a). In the case of MoS_2, the upper theoretical limit, computed by density functional theory calculations, for μ at room temperature (dominated by phonon scattering) is about 400 cm^2 V^{-1} s^{-1} (ref. 76), whereas the experimental results so far are in the range of few tens of cm^2 V^{-1} s^{-1} (refs 77,78). Recent results[79,80] have shown that few-layer phosphorene (a 2D lattice composed of phosphorus atoms) has a μ of 286 cm^2 V^{-1} s^{-1} (ref. 79), which increases up to ~1,000 cm^2 V^{-1} s^{-1} as the number of layers are increased to form a film with a thickness of about 10 nm (ref. 80).

The ultimate thin body of TMDs has a strong impact on device scaling prospects. For example, Liu *et al.*[81] have shown that MoS_2 FETs can comply with the ITRS down to a minimum channel length of 8 nm, whereas silicon MOSFETs can go down to a channel length of 10 nm with UTB of 3 nm. For such aggressively reduced geometries, the low MoS_2 μ is not a real issue, because transport can be considered as almost ballistic. Similar considerations apply to other TMDs with comparable energy gap and carrier effective masses.

Within the ballistic regime, the large relative effective mass for electrons and holes in TMDs, between 0.56 and 0.66 for all carriers

Table 1 | Main FoM extracted from ITRS[7] for the current (2014), mid- (2018) and long-term (2026) nodes for both high-performance (HP) and low-power (LP) technologies.

	HP2014	LP2014	HP2018	LP2018	HP2026	LP2026
Channel length (nm)	18	19	12.8	13.1	5.9	5.8
V_{DD} (V)	0.82	0.65	0.73	0.57	0.57	0.43
I_{off} (nA μm^{-1})	100	5	100	5	100	5
I_{on} (μA μm^{-1})	1,573	765	1,805	794	2,308	666
DPI (fJ μm^{-1})	0.47	0.29	0.31	0.18	0.14	0.07
τ (ps)	0.361	0.58	0.24	0.4	0.1	0.26
I_{on}/I_{off}	15,730	153,000	18,050	158,800	23,080	133,200

V_{DD} is the supply voltage; I_{off} and I_{on} are the currents in the off and in the on state, respectively; DPI is the dynamic power indicator; τ is the intrinsic delay time; and I_{on}/I_{off} is the ratio between the on and the off currents.

in MoS_2, $MoSe_2$, $MoTe_2$, and 0.34 for electrons and 0.44 for holes in WS_2 (ref. 82), represents an advantage over traditional semiconductors. Indeed, a larger effective mass implies a larger density of states and therefore a larger ballistic I_{on}, which is proportional to the square root of the product of the longitudinal and the transverse in-plane effective mass[83]. Moreover, a larger effective mass means a reduced source–drain tunnelling component[84], which would degrade the SS and increase I_{off} (indirectly reducing I_{on}, as gate work-functions are chosen to match a given I_{off}). Electrons and holes in silicon and III–V materials have smaller effective masses (for example, 0.29 for Si and 0.15 for GaAs) than TMDs, with silicon having the advantage of two degenerate minima.

Taking into account the above facts, TMD-based FETs compare favourably with the expectations of the ITRS for high-performance logic devices. For example, let us consider the ITRS requirements for high-performance devices for 2023 (supply voltage of 0.62 V, gate length of 8.1 nm, I_{off} of 100 nA μm^{-1}). In the best-case scenario of ballistic transport, a MoS_2 FET would exhibit a delay time of 60 fs (ref. 81), which is much smaller than that of a silicon MOSFET according to the ITRS[7]. This is against a minimum ITRS requirement of 140 fs (ref. 7), well beyond expectations for silicon MOSFETs. Similar considerations hold for other TMDs, which share similar carrier effective masses.

As of now, there are no reported data on high-frequency operation of devices and circuits based on TMDs. Experiments have, however, demonstrated the operation at low frequency (a few kHz) of a simple CMOS inverter and NOR port[85], a ring oscillator[86] and a static random-access memory cell[86]. Device optimization and fabrication for high-frequency operation have not been addressed yet.

In Fig. 4b we compare the theoretical and experimental FoM of MoS_2 FETs with ITRS 2012 predictions for high-performance logic, and with selected theoretical[87] and experimental[88] results on III–V MOSFETs. On the one hand, experimental results on MoS_2 FETs[85,86] and on III–V FETs[69] are far worse than CMOS state-of-the-art, in terms of intrinsic delay time, and are closer in performance to CMOS technology of the early 1990s. On the other hand, theoretical results for MoS_2 FETs with gate lengths of 8.1 and 5.9 nm (ref. 81) and with 12-nm III–V FETs[69] are promising with respect to the ITRS expectations[7]. Current experiments using TMDs have not yet addressed channel length scaling, from which most of the performance improvements are foreseen. Indeed, considering a channel length below 10 nm, carrier transport becomes quasi-ballistic[81]. In Fig. 4c, the delay time of inverters is plotted as a function of transistor gate length. For long (>μm) channel devices, graphene inverters outperform inverters based on MoS_2, carbon nanotubes (CNTs)[89,90] or polymers[91], and deliver delay times comparable to those offered by silicon[92,93]. To meet the requirements set by the ITRS for future nodes, scaling down the gate length is urgently needed, setting the focus of future research on 2DM-based devices and circuits.

Low-power devices. To significantly outperform existing Si-based low-power CMOS, devices with SS <60 mV dec^{-1} are needed. One of the leading transistor candidates, able to work at low voltage and with a low SS, is the tunnel field-effect transistor (TFET)[66,94]. The TFET achieves low SS by replacing the field-controlled barrier lowering mechanism of the MOSFET by field control of band-to-band tunnelling[66,94]. The experimental state-of-the-art of TFETs has been recently assessed[95]. A summary of the experimental results is shown in Fig. 4d, which plots the measured TFET SSs as a function of drain current. Subthreshold swings of less than 60 mV dec^{-1} have been reported for a wide variety of materials including CNTs[96,97], Si (refs 98–100), SiGe (ref. 101), Ge (ref. 102), Ge/Si (ref. 103), InAs/Si (ref. 104) and InGaAs (ref. 105). There are no reports of low SS TFETs made of TMDs. In the absence of experimental results, the projected TFET performance for 2DMs (Fig. 4d) is based on simulations by Ghosh and Mahapatra[106] and by Zhang and colleagues[107]. These simulations provide the first estimates of the potential of 2DM-based TFETs with respect to the state-of-the-art devices. Moreover, the results of the simulations represent an upper limit for the performance to be expected from TMD-based devices, as they neglect tunnelling via interface states, as well as parasitic source-to-drain resistances[106,107].

The motivation for the exploitation of 2DMs for TFETs has recently been discussed by Jena[108] and Das and colleagues[109]. Two-dimensional materials provide a fully terminated surface, free of dangling bonds. Dangling bonds lead to surface states and traps in bulk semiconductor materials, which are detrimental to the SS. There are many TMDs with energy bandgaps in the range of interest (~1–2 eV) for scaled low-power devices. These bandgap values can provide the thermal barriers needed to achieve beyond-CMOS off currents. Tunnel junctions in bulk semiconductors are often defined by forming abrupt p–n junctions. The doping densities that can be achieved are limited by the solid solubility of the dopant atom in the crystal and this limits internal electric fields to, for example, about 2–3 MV cm^{-1} in Si (ref. 110). Two-dimensional materials have the potential to raise these internal fields significantly, using modulation doping or ion doping. Ion doping in graphene has been shown to induce electron and hole sheet densities exceeding 10^{14} cm^{-2} (ref. 111). Thus internal fields greatly exceeding the limits of bulk tunnel junctions are feasible, allowing much higher current densities. Figure 4e shows the computed tunnel currents for TMD homojunctions plotted against electric field for a wide range of TMDs[112], as well as the I_{on} target for CMOS low-power transistors, summarized in Table 1.

In addition to the TMDs, ultrathin Bi_2Se_3 has been demonstrated experimentally to behave like a semiconductor with a bandgap of 250 meV (ref. 113). Atomistic simulations have shown the potential of Bi_2Se_3 for low-power applications, showing large I_{on}/I_{off} ratio with V_{DD} = 0.2 V (ref. 107), as well as good performance in MOSFET devices, but hindered in part by the large dielectric constant[114].

Transition metal dichalcogenides have strong potential for UTB-FETs for low-power applications where their strength relies on the high I_{on}/I_{off} ratio, 10^{10}, with a SS approaching 60 mV dec^{-1} (refs 115,116). For low-power devices with ultrashort channel (5 nm), Alam and Lake[117] have demonstrated that MoS_2 FETs show better performance characteristics than the UTB silicon counterpart.

Although many of the 2DMs such as TMDs hold promise over conventional semiconductors (Si, ref. 118; and III–V, refs 119–123) as the ultimate UTB-FET in terms of electrostatics, appropriate n- and p-type dopants still need to be identified and studied. Instead, adsorbates or native chalcogen vacancies are used for charge transfer doping[124]. Furthermore, the contact resistance issue, as discussed above, is of paramount importance[58].

The possibility of having symmetric conduction and valence bands[8] in 2DMs such as graphene opens the way for the realization of new device concepts. It has been proposed that resonant tunnelling can be observed in materials with symmetric band structure[125]. In particular, negative differential resistance has been demonstrated through simulations[126] and also proven experimentally by Britnell and colleagues[127].

Analog and RF applications

High-frequency electronics is currently dominated by III–V and SiGe-based semiconductor transistors with the highest reported f_{max} values in the range of 1–2 THz, enabling simple circuits to operate up to a few hundred gigahertz. These technologies are very mature, and there is only a small margin left to increase speed further. However, the growing demand for larger bandwidth in communication systems and new sensor applications will require devices to extend the operating frequency deep into the terahertz regime[128].

Geometric and parasitic capacitance scaling, high μ and saturation velocity are the keys to boost device speed. From this perspective, we believe that RF is the only electronic application where graphene can play a relevant role, having shown the highest μ (refs 129–131) and saturation velocity[132–134] of any FET channel material so far. To some extent, graphene transistors have already fulfilled these expectations by delivering intrinsic f_T comparable to the best available III–V transistors and surpassing Si-based transistors at comparable gate lengths[135]. Further, the limit of f_T, well beyond 1 THz, has been predicted through simulation for these transistors but has yet to be demonstrated experimentally, and if achieved would significantly surpass other technologies[136].

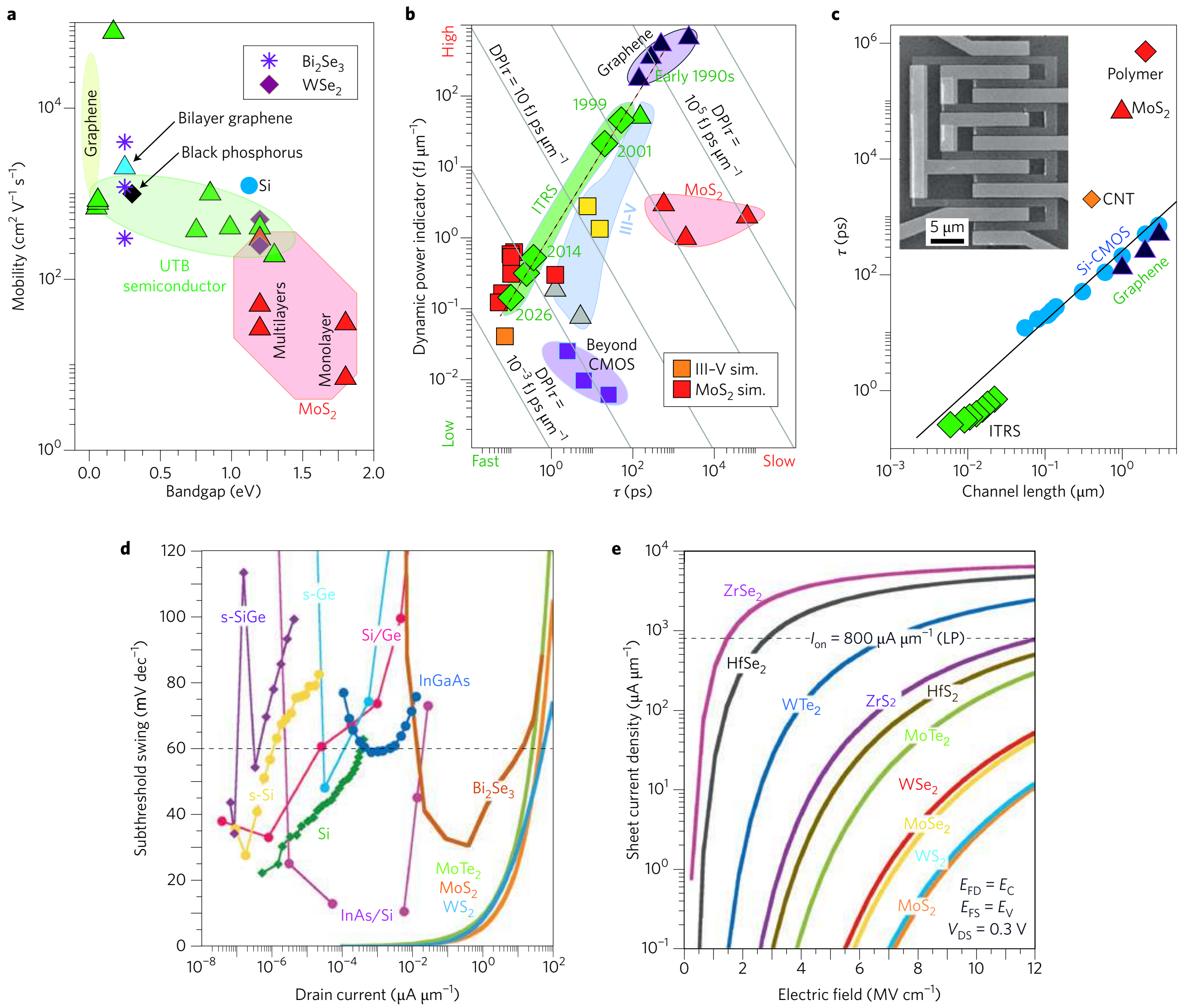

Figure 4 | Figures of merit of two-dimensional materials for high-performance and TFET applications. a, Mobility versus bandgap for different semiconductor materials. Green triangles, data from refs 118–123; red triangles, refs 77,78,142,143; blue circle, ITRS[7]; black rhombus, ref. 80; cyan triangle, ref. 139; purple asterisks, ref. 113; purple rhombuses, refs 71,72. Graphene data are taken from refs 63,74,75. **b**, Dynamic power indicator (DPI) and τ for different technologies and ITRS[7] requirements. Square symbols refer to simulation, triangles to experimental results. Red squares, data from refs 81,115,116; orange square, ref. 81; yellow squares, ref. 87; purple squares, ref. 15; grey triangles, ref. 69; red triangles, refs 16,86; green triangle, ref. 88; black triangles, refs 149,150; green rhombuses, data extracted from ITRS[7] for the different technological nodes with the corresponding year also highlighted. Oblique lines are the isolines of the product DPIτ, which represents a figure of merit accounting at the same time for both energy dissipation and device speed. Dashed line is the line best fitting the data extracted from ITRS for the different technological nodes. **c**, Switching time of an inverter, τ, driving an identical inverter (fan out 1, where fan out is the number of digital inputs that the output of a single logic gate can feed), for inverters based on different materials as a function of gate length. Red rhombus, data from ref. 91; red triangle, ref. 86; orange rhombus, ref. 89; black triangles, ref. 149; green rhombuses, data extracted from ITRS[7]; blue circles, refs 92,93. The straight line is a guide to the eye. Inset: An optical micrograph (courtesy of Roman Sordan, Politecnico di Milano) of a five-stage graphene ring-oscillator. **d**, Measured subthreshold swing (SS) as a function of drain current for experimental tunnel field-effect transistors versus simulations from Ghosh and Mahapatra[106] (courtesy of Hao Lu, Univ. of Notre Dame). Violet rhombuses, data from ref. 101; cyan dots, ref. 102; red dots, ref. 103; green rhombuses, refs 99,100; purple dots, ref. 104; yellow dots, ref. 98; blue dots, ref. 105; brown line, ref. 107; dark cyan, orange and green lines, ref. 106. The dashed line refers to the lowest SS achievable in thermionic devices, that is, SS = 60 mV dec^{-1}. **e**, Simulated tunnel current density in abrupt TMD p–n junctions versus junction electric field and compared with low-power CMOS targets from ITRS[7] in Table 1. The dashed line refers to the I_{on} required for low-power (LP) applications for ITRS 2018 (courtesy of Nan Ma, Univ. of Notre Dame).

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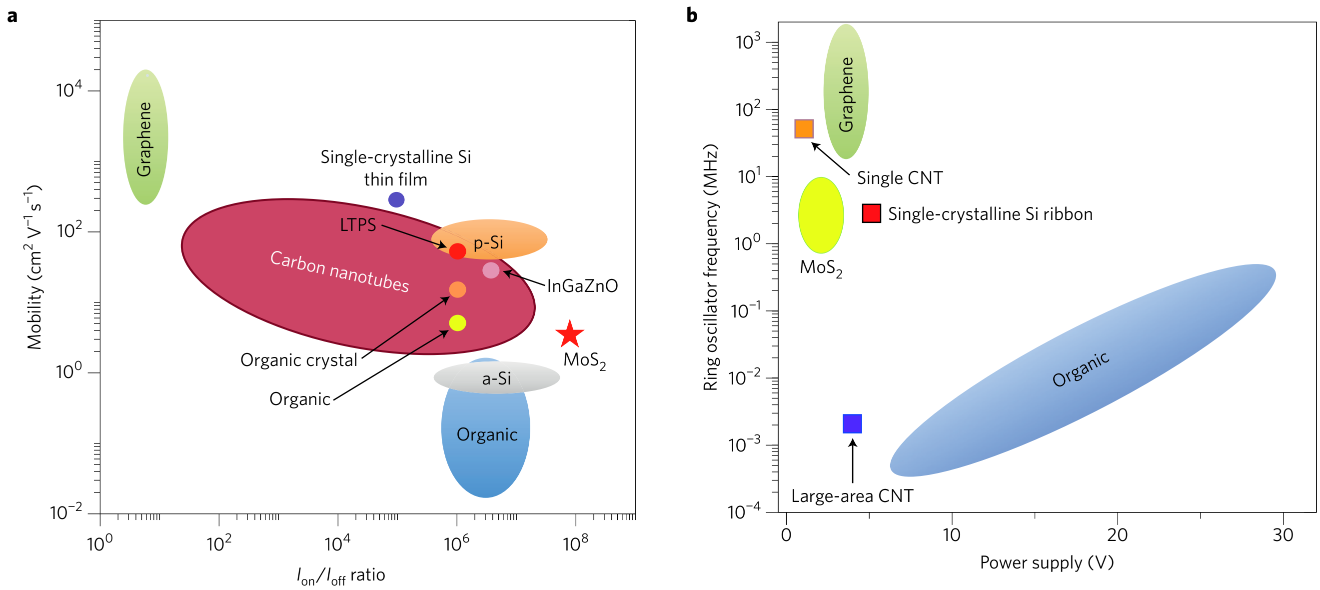

Figure 5 | Figures of merit of transistors for flexible electronics. a, Trade-off between μ and I_{on}/I_{off} ratio for materials typically used in flexible electronics. Purple dot, data taken from ref. 193; red dot, ref. 172; orange dot, ref. 169; yellow dot, ref. 169; grey dot, ref. 194; red star, ref. 86. Graphene data are taken from refs 30,60,153; CNT from refs 178–180; p-Si from refs 173,174; a-Si from ref. 195; organic semiconductors from ref. 168. **b**, Operating frequency and voltage of ring oscillators made of flexible semiconductor materials. Data in orange square are taken from ref. 89; red square, ref. 165; purple square, ref. 181. Graphene data are taken from refs 149,150; MoS_2 from ref. 86; and organic semiconductors from ref. 91. LTPS, low-temperature polycrystalline silicon.

However, as stated above, rather than f_T, much more attention needs to be paid to f_{max}. From this point of view, graphene transistors still lie behind III–V and Si-based transistors, and the route for filling the gap has not been paved yet[135]. So far, the highest reported f_{max} of a graphene transistor is 90 GHz (ref. 137), whereas InP transistors have achieved 1.2 THz (ref. 138). A reduction of the still large parasitic effects in these devices (that is, contact and/or gate resistance) is urgently needed to increase f_{max} significantly (equation (1)). It is still unclear, though, whether these improvements will be sufficient to improve f_{max} beyond the threshold of 1 THz. In particular, the absence of a bandgap in graphene may prevent proper current saturation, especially at the required[7] short gate lengths[139]. Thus, introducing a bandgap in graphene is a promising route[139] and simulations for bilayer graphene-based FETs predict f_{max} values well beyond 1 THz (ref. 140). However, the introduction of a bandgap comes at the cost of reduced μ (ref. 141). Nevertheless, although graphene-based RF transistors are predicted to perform significantly better than III–V materials[140], they still need to be supported by experimental evidence. Therefore, it will be crucial for the success of graphene-based RF transistors if the aforementioned parasitic effects can be significantly reduced, coupled with current saturation at short gate lengths (smaller than 30 nm).

Other 2DMs such as MoS_2 show pronounced current saturation and therefore could provide a good alternative to graphene[86]. However, the μ and saturation velocity in MoS_2 are significantly lower not only than in graphene (Fig. 2), but also than in Si and III–V materials[77,78,142,143]. Hence, high operation frequencies are unlikely to be achieved using MoS_2 as the channel material for FETs. On the contrary, Bi_2Se_3 has been demonstrated to offer significantly higher μ (20,000 cm^2 V^{-1} s^{-1})[144] than MoS_2 (ref. 16) but other important material properties, such as saturation velocity, and device scalability are still unknown, making it hard to predict their potential in this field.

Besides FETs, different transistor geometries have been proposed and realized, including vertical tunnelling transistors[127,145], utilizing heterostructures of different 2DMs, and ballistic devices[146–148]. These device architectures have the potential to make terahertz frequencies accessible, without struggling with the gapless nature of graphene. Although few experimental data are available at present on these devices, especially for RF operation, this scenario is likely to change rather soon, as the future progress in this promising area will benefit greatly from the huge amount of work being performed on optimizing process technology for graphene-based FETs.

Moving from single devices to integrated circuits requires reproducibility of the device technology and involves a more complex fabrication process. It is therefore not astonishing that the realization of integrated circuits based on 2DMs is still in its infancy, with the proposed integrated circuits[86,149–158] delivering mainly proof-of-principle operation. So far, voltage amplifiers[149,152], mixers[153–155], frequency doublers[149,152,158], oscillators[86,149,150] and combinations of those[159] have been realized using mainly graphene and in part also MoS_2-based FETs, covering the major active building blocks of modern electronics. The corresponding operation frequency of graphene-based circuits is comparable to those based on silicon, having transistors with similar gate lengths, as illustrated in Fig. 4c for the case of single inverters in ring oscillators. However, all of the aforementioned circuits use long channel transistors with a physical gate length of at least a few hundred nanometres and are therefore unable to compete with the latest circuits based on scaled III–V and Si–Ge transistors.

New functionalities have instead been obtained that make use of the ambipolar nature of graphene, in particular for circuits relying on the nonlinear response, such as mixers and frequency doublers. Circuits based on graphene[122,158] and bilayer graphene[125] FETs[153,156] have already shown excellent performance compared with established technologies.

Although existing mature semiconductor technologies benefiting from multi-billion dollar investments continue to improve, the unique properties of 2DMs and the large performance improvements made in the past few years predict an exciting future where integrated circuits based on 2DMs could surpass the performance of established technologies, opening opportunities for new applications.

Table 2 | Summary of the opportunities and challenges for 2DM-based electronics in different applications.

	Opportunities	Challenges
Production	Uniform single-crystal films Inexpensive fabrication technology High mobility Atomically thin films 2DM-inks with on-demand electronic properties	Reduction of surface states Growth of large (>1 cm^2) single crystals Doping control (less than the solubility limit) Metal/semiconductor interface control On-demand control of morphological (lateral sizes and thickness) and rheological (surface tension, viscosity, density) properties of 2DM-based functional inks
High performance	Reduced short-channel effects Good performance in terms of τ, I_{on}/I_{off} (>10^4)	Fabrication of ultrashort channel devices (channel length smaller than 10 nm) Fabrication of devices based on new principles to reduce V_{DD} and SS Good ohmic contacts with low source–drain parasitic resistance
Low power	Low-power performance as compared with Si (power supply <0.5 V) Good control of the gate over the tunnel barrier, with SS << 60 mV dec^{-1} Large I_{on} currents (>10^3 μA μm^{-1})	Fabrication of doped tunnel junctions Low interface states to reduce SS Design of new device architectures
Radiofrequency	High μ and saturation velocity (graphene) Development of 2DM heterostructures for terahertz operations	Reduce contact resistance (<100 Ω μm) Obtain f_{max} in the THz range
Flexible electronics	Ultrathin bendable material Mobility larger than in materials already available (>40 cm^2 V^{-1} s^{-1}) Enabling technology for wearable electronics	Improve material mobility Development of roll-to-roll fabrication processes Development of device/circuit fabrication technologies

Flexible electronics

Numerous applications demand the development of large-area, flexible and conformal electronics. For example, wearable electronics[160] require flexible displays, the cost of installing photovoltaic panels could be significantly reduced through the use of roll-to-roll processes, and 'skin tattoos' with embedded electronic devices and sensors[161] could revolutionize healthcare.

However, there are several challenges limiting the traditional approaches for flexible and large-area electronics. Conventional Si circuits can be made flexible by thinning down the Si wafer below 25 μm (refs 162–165). Although this approach allows the use of state-of-the-art Si technology in flexible applications, the brittle nature of Si imposes limitations on the lifetime and reliability.

Other technologies for flexible large-area electronics, such as organic semiconductors suffer from very poor transport properties, where μ values are typically well below 10 cm^2 V^{-1} s^{-1} (refs 166–170; Fig. 5a). These low μ values increase the on resistance of the devices, thereby reducing their current driving capability and their operating frequency. Furthermore, high voltages are needed to drive the required high current levels, which increase the complexity of the circuits (Fig. 5b). Polycrystalline silicon (micrometre-sized grains) on the other hand, despite its relatively high mobility (~100 cm^2 V^{-1} s^{-1})[171–174], requires complex technological processes, and suffers from large leakage current, poor yield and high cost when processed at the low temperatures (<120–150 °C) needed for flexible plastic substrates, for example, polyethylene terephthalate or polyethylene naphthalate.

Two-dimensional materials, in general, could be an ideal choice for future flexible electronics[46]. They tend to have excellent mechanical properties[175–177], can be prepared in polycrystalline form over large areas, can be transferred to arbitrary substrates making them mechanically compatible with flexible device fabrication, and unlike CNTs[178–181] do not require any sorting process[182–184]. At the same time, the transport properties of 2DMs[185] (that is, μ), when grown over large areas by CVD, can be orders of magnitude higher than for materials used at present, such as organic semiconductors[166,167], thus enabling higher frequency at low power (Fig. 5). Finally, the large number of 2DMs provides a wide selection to choose from for device optimization.

Although the development of 2DM-based flexible electronics is still in its early stages, several promising demonstrations have already been reported[50,176]. Circuits have been fabricated on 2DMs transferred to flexible substrates such as polyethylene naphthalate[186,187], and TMD-based devices have also shown I_{on}/I_{off} ratios of 10^4 after flexing to a bending radius of 0.75 mm on a polymer substrate[176], using both Al_2O_3 and HfO_2 gate dielectrics[188], up to strains of 1.5%, while maintaining mobility up to about ~45 cm^2 V^{-1} s^{-1} (ref. 13).

Many of the applications of interest in flexible electronics involve chemical[189] and biological[190] sensors, for which exciting demonstrations already exist. For example, Mailly-Giacchetti *et al.*[189] developed a graphene-based pH sensor on a flexible polyethylene naphthalate substrate in which variations in the pH changed the current flowing through a graphene transistor with an electrolyte gate. Graphene was also used as the antenna/transceiver of a wireless bacteria detection system on tooth enamel[190]. In this system, graphene was printed onto bioresorbable silk and contacts were formed on a wireless coil. As the analyte of interest is adsorbed on the graphene surface, the resistance of the graphene layer changes, and this is wirelessly monitored using an inductively coupled RF reader device. A detection limit down to a single bacterium has been demonstrated in this remotely powered sensor[190].

Summary remarks

There is no question that the electronics industry, as in the case of the vacuum tube nearly 70 years ago, would benefit from the replacement of the current transistor with a switch that uses much lower power. This lower power switch could re-energize the electronics industry, accelerate its growth and lead to portable products that are impractical today. The question that faces us today is, "Do we have the right new materials and devices that will enable the industry to develop new low-power systems with the potential of revolutionizing the industry?" There are many groups around the world evaluating different approaches to this problem, and 2DMs are at their centre. Table 2 summarizes some of the opportunities and challenges discussed in this Review.

The main opportunities for 2DMs for both high-performance and low-power applications stem from the ultimate thinness achievable in 2DM-based devices, which lead to an almost perfect control of the channel potential. Such a property can be fruitfully exploited both in UTB-FETs and in TFETs, to reduce the power consumption in integrated circuits, which is the biggest limiting factor of electronics today. It must be recognized, however, that there are caveats and challenges. Although the channel material itself may be atomically thin, electric field lines can extend from the drain to the source through the underlying buried oxide, leading to drain-induced barrier lowering, or through the high-*k* gate dielectric, leading to so-called fringing-field-induced barrier lowering. Low-specific-resistance ohmic contacts to these materials are also a tremendous challenge, and parasitic series resistance will become more limiting as channel lengths are scaled down. Also, high-*k* gate dielectrics with low interface defects density on such materials are yet to be developed.

Processing of 2DMs in general is in its infancy, and the community is attempting to establish baseline properties[191] by using micromechanical cleaving and comparing them with films grown by more production-worthy techniques such as CVD and MBE. Before these production processes can be used in any high-volume manufacturing environment, the growth conditions that yield high-quality films need to be established and optimized. Furthermore, layer control, point- and line-defect control, development of ohmic contacts, and appropriate n- and p-type dopants need to be identified and studied. Nowadays, graphene single crystals can be reproducibly grown up to about 1 cm^2 in diameter on a Cu substrate, and recently single-crystal graphene up to 5 cm in diameter was grown on germanium (110)[192], but there are still many challenges ahead in creating very 'flat' (<0.2 nm surface roughness) two-dimensional films of any kind. Much effort will have to be dedicated by industry and the research community alike to achieve films with these properties.

If large-area materials growth is successful, 2DM technology could enable a new generation of flexible electronics for wearable and bendable systems. The requirements for these systems are different for high-performance and low-power applications. It is important to maximize the I_{on}/I_{off} ratio and develop cost-effective large-area fabrication techniques. By enabling ubiquitous electronics in walls, fabrics or windows, 2DMs would be creating completely new markets for the electronics industry, rather than competing with or trying to displace existing well-established technologies to provide higher performance. Researchers from universities and industry alike argue that this is probably an easier road towards the first application of these truly amazing materials.

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Competing financial interests

The authors declare no competing financial interests.

ERRATUM

Electronics based on two-dimensional materials

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In the version of this Review Article originally published, in Fig. 4c, the *y*-axis values were incorrect; they should have been '10^0, 10^2, 10^4 and 10^6' (from bottom to top). This error has now been corrected in the online versions of the Review Article.