

INTRODUCTION

From the designer, to the foundry, the consumer, microchips go through a lengthy process which has lots of risk spread throughout. The most vulnerable moment for a microchip begins straight out of the designer's workshop, when the logic gates inside the chip can be tampered or altered.

Several methods revolving around the concept of **logic locking** have been introduced in order to combat this. Logic locking is a general method which integrates **keys** in the form of extra logic gates. If an illegal user feeds a wrong key value, the chip will be "locked", which means it will function incorrectly.

During our research, we applied **random logic locking (RLL)**, which randomly inserts XOR/XNOR gates across the circuit. To evaluate the attack resilience of this technique, we used a tool called NEOS. Furthermore, we explored the possibility of training a **graph neural network (GNN) model** to predict the attack resilience of any locked circuit.

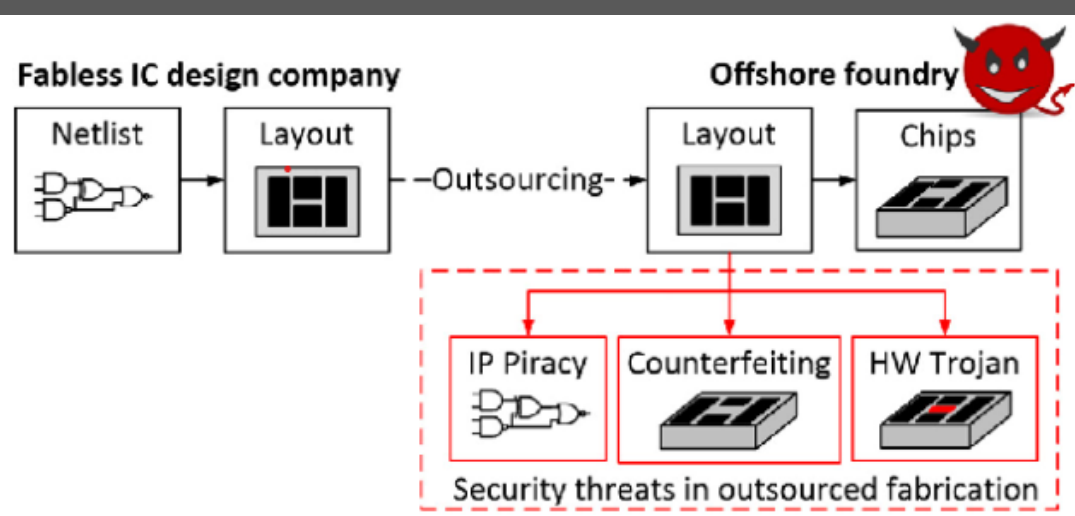


Figure 1: Security threats in outsourced fabrication

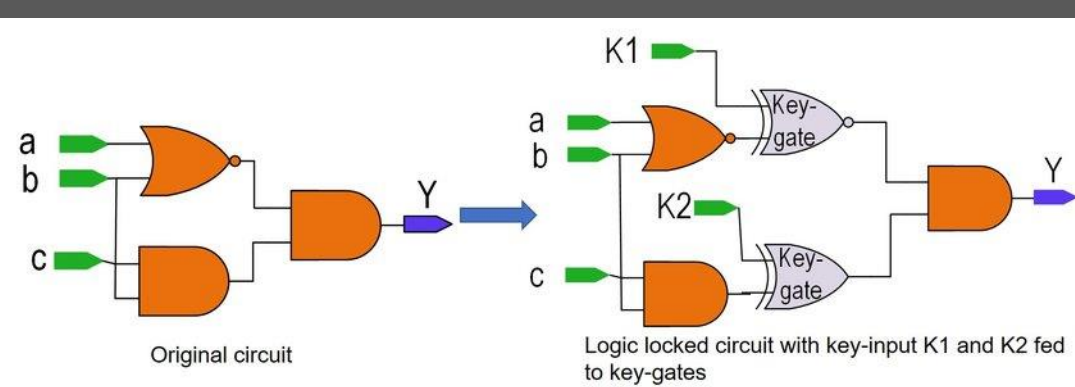


Figure 2: (left) non-encrypted; (right) encrypted with XNOR/XOR gates

SKILLS LEARNED

- Dataset creation and machine learning model training
- Gate-level digital circuit design
- Navigation and utilization of Linux server
- Test environment setup (Anaconda, NEOS, ABC, OGB)
- Advanced Python techniques



LEARNING PROCESS & RESEARCH

In order to understand what was going on behind the scenes, I started by learning how **logic gates** work.

After studying circuit composition, I delved into intensive research on various **machine learning models and algorithms**, each serving different purposes. These models consist of layers that utilize complex mathematics to produce the correct function. One prevalent model we focused on is the **GNN**.








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| Truth Table | <table><tr><th>A</th><th>X</th></tr><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></table> | A | X | 0 | 1 | 1 | 0 | <table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table> | B | A | X | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 | <table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> | B | A | X | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | <table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table> | B | A | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | <table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> | B | A | X | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | <table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> | B | A | X | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | <table><tr><th>B</th><th>A</th><th>X</th></tr><tr><td>0</td><td>0</td><td>1</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></table> | B | A | X | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
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Figure 3: The Boolean truth tables for logic gates

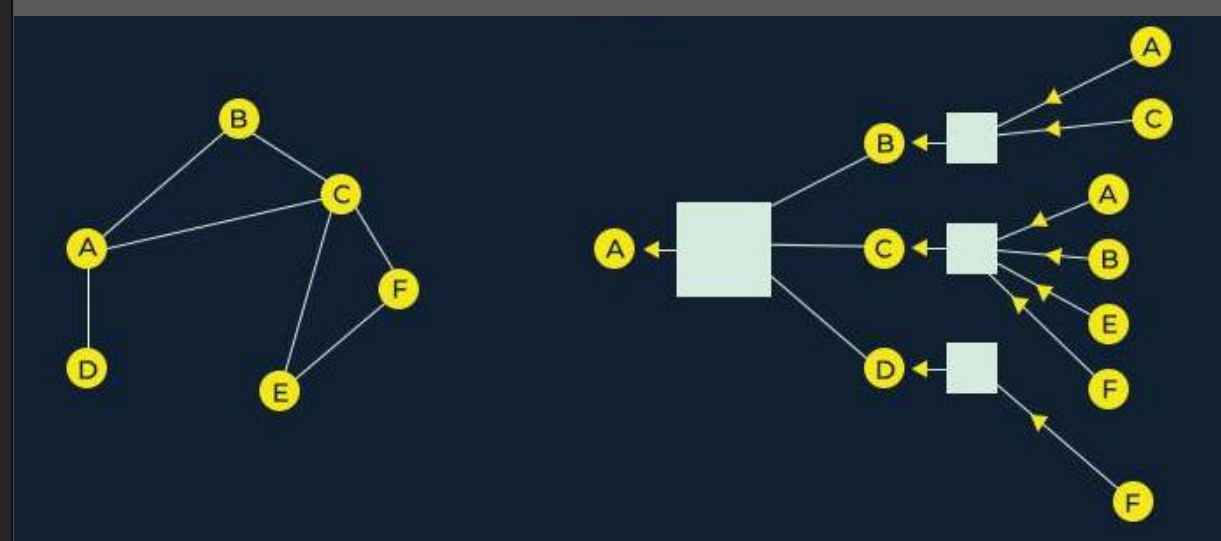


Figure 4: A basic representation of a GNN

METHOD

1. Use RLL to encrypt original circuits with different key lengths
2. Use NEOS to break locked circuits and collect the attack runtime
3. Generate a dataset including node features and graph labels
4. Train a GNN model using the dataset
5. Evaluate the performance using root mean squared error (RMSE)

$$RMSE = \sqrt{\frac{\sum_{i=1}^N (pred_i - actual_i)^2}{N}}$$

```

1 INPUT: graph, filename, and circuitname
2 OUTPUT: 6 written csv files
3
4 Open 6 files
5 EdgeFeat, GraphLabel, NodeFeat,
6 Edge, NumNodeList, NumEdgeList
7
8 Then open Master file and read GraphLabel
9 for line in line:
10     readLine line in Master
11     writeLine line in GraphLabel
12
13 For nodename in graph.nodes:
14     open NodeFeat:
15     writeLine nodename in NodeFeat(
16     gatetype, fanInCone, fanOutCone
17     )
18
19 Create index dictionary
20 For node in graph:
21     index[node] = i
22     i++
23 For edgenames in graph.edges:
24     writeLine index(i,i+1) in Master
25
26 In NumEdgeList writeLine len(graph)
27 In NumNodeList writeLine len(graph.edges)
28 Close all files

```

RESULTS & CONCLUSION

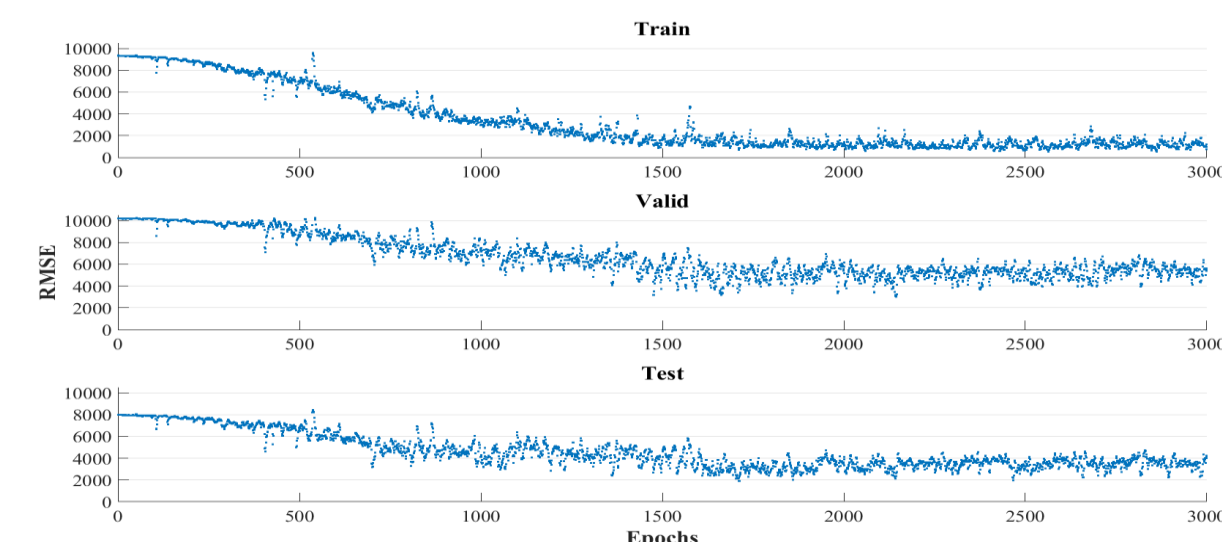


Figure 4: Scatter plot graph of training results, validation results and test results

We generated a dataset of 124 encrypted circuits, and use the gate type, size of fan-in cone, and size of fan-out cone as the features for training. We attack them with a timeout of 4 hours (14400 seconds) and use the attack runtime as the graph label. In the plots above, the x-axis represents the number of epochs, and the y-axis is the value of RMSE. After training, the model can also realize a similar accuracy in the test dataset, which exhibit the generalization of our model.

Next Steps

1. In order to gain more consistent and applicable results, introducing more original data to encrypt would be beneficial to the model's long-term success. Additionally, changing the way we encrypt the circuits could benefit the way our model learns over time.
2. There is a big fluctuation in test curve. We are going to apply different solutions, including increasing the proportion of test dataset, tuning the hyperparameters of our model, and adding more features.

ACKNOWLEDGEMENTS

I wish to express my utmost gratitude to Professor Pierluigi Nuzzo, whose unwavering kindness and infectious enthusiasm have revealed the sheer excitement and captivating nature of pursuing one's passion.

I am forever indebted to Kaixin Yang, my esteemed mentor, whose invaluable guidance and unwavering support have fundamentally transformed my life and bestowed upon me a fresh perspective.

And Thank you to Matthew Ai and Marcus Gutierrez, who have always demonstrated their support and availability.