

# **GNN-Powered Circuit Delay Estimation** Steven Shi | stevenshi15@gmail.com **DesCyPhy Lab** Arcadia High School, Class of 2024 **USC Viterbi Department of Electrical Engineering, SHINE 2023**

## **Skills Learned**

In a world that relentlessly pursues faster and more advanced computers, the demand for superior chips has only intensified. Area, power consumption, and delay are among the essential aspects of a well-performing circuit. Area and power consumption exhibit a directly proportional relationship with the fundamental building blocks of modern circuits, known as gates. However, the delay of a circuit exhibits a nonlinear association with the gate count, making it considerably more challenging to accurately predict.

Introduction



Figure 1. Diagram showing the process of estimating a circuit's delay



Nevertheless, by harnessing the power of Graph Neural Networks (GNNs), it becomes conceivable to estimate the delay of a circuit. In our research, our objective is to leverage GNNs to estimate the delay of a circuit, thus contributing to the advancement of circuit design and optimization.

## **Objective & Impact of Professor's** Research

One of Professor Nuzzo's research areas is the obfuscation of integrated circuits to enhance their protection, encompassing formal foundations, analysis, and design methods for hardware IP protection.



Figure 2. Generic functional model for logic locking

Before commencing the research, I familiarized myself with the background information of my project. The subject matter was divided into two main categories: circuits and graph neural networks (GNNs).

I took the time to familiarize myself with the different elements of circuits, particularly the logic gates that form the foundation of each circuit. I learned how each gate functions, as well as the concepts of sequential and combinational logic. Additionally, I explored finite state machines and gained an understanding of Verilog, a hardware description language commonly used in the field.



I studied graph neural networks (GNNs) and graph convolutional networks (GCNs), gaining a deep understanding of the linear algebra behind transforming data for machine learning. I also explored activation functions like ReLU that help the model find patterns in the data. Additionally, I learned about how to use dropout to prevent overfitting and the mathematical foundations of weight and bias updating through backpropagation.



Figure 4. Example of the calculus behind backpropagation

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## **Methods and Results**



Figure 5: Diagram of how a GNN works

Following extensive experimentation involving diverse dataset sizes and hyperparameters, we have unveiled a remarkable revelation: our model has achieved a commendable test Root Mean Squared Error (RMSE) value of approximately 0.15. Moreover, during the meticulous assessment of its accuracy, we observed a mean absolute percentage error of 0.05. In essence, these compelling results unequivocally demonstrate that our model possesses an outstanding ability to predict circuit delays with an impressive accuracy of up to 95%.

To initiate our research, we opted to utilize Open Graph Benchmark(OGB), which offers baseline scripts for graph property prediction tasks. We formatted our data to meet the required specifications and began by testing the model on 17 circuits. Subsequently, we progressed to a larger dataset comprising 450 circuits. We segregated our data into three distinct sets: one for training purposes, one for validating and fine-tuning hyperparameters, and one for assessing the model's accuracy. To optimize our model's performance, we carefully adjusted key parameters, setting the learning rate at 0.001 and the dropout rate at 0.25.



Figure 6. Graph with the accuracy of our model

## Citations

Weihua Hu et al. "Open Graph Benchmark: Datasets for Machine Learning on Graphs". In: arXiv preprint arXiv:2005.00687 (2020).

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